

GEMINI

Near Infrared Coronagraphic Imager (NICI)

Dual Array Controller Electronics Specification GEMINI SDN3003

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PRELIMINARY

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1 Dual Array Controller Overview

This document provides a subsystem level description of the array control portion of the Gemini NICI instrument. This document has been created to account for configuration and implementation details specific to the NICI project.

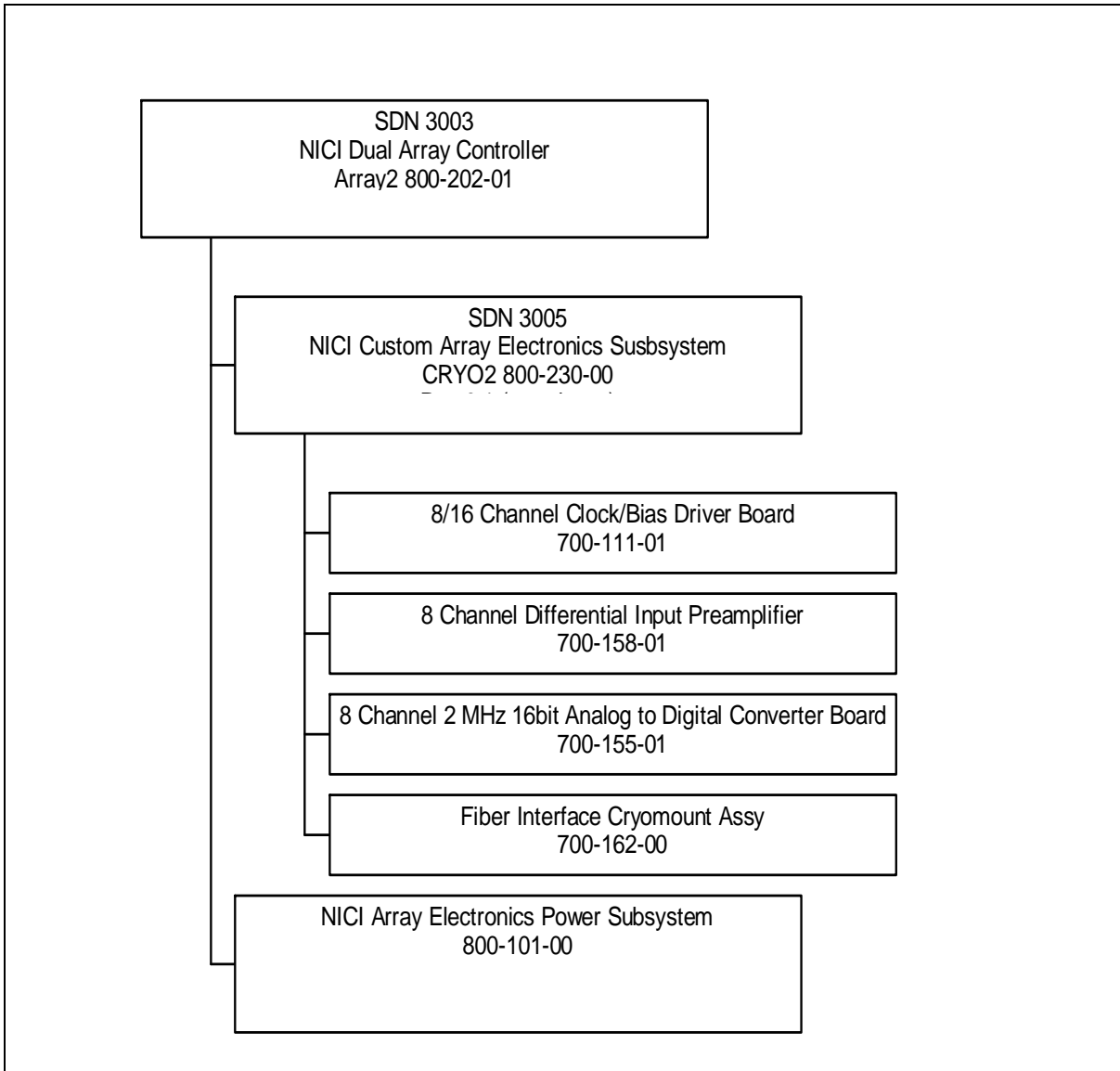
The main goal of the NICI project is to enable imaging of faint regions in the immediate vicinity of bright sources. The Dual Array Controller is dual implementation of MKIR's Redstar3 Array Controller. The Redstar3 provides control of and data acquisition from a four quadrant Aladdin type III 1024x1024 array. By using both of these channels one can observe in a differential mode and high fidelity frame differencing is possible.

Clocking control of the arrays are provided by digital clock signals converted to analog levels and fed to the array in the cryostat. The resulting array outputs are amplified and converted to digital pixel data. The pixel data is passed over a high speed fiber link to server class multiprocessor computers called Pixel Servers. The Pixel Servers can perform preliminary data processing and store the data locally or pass the data on to Gemini's Data Handling System (DHS).

Frame readout and co-addition rates are capable of up to 10 Hz frequency with synchronization accuracy between the arrays of 1 millisecond. The Dual Array Controller can operate in standalone mode or under Gemini Facility control in remote mode. Read noise is limited to a 10% increase by the controller.

The two channels in NICI are referred as Red and Blue channels.

2 Subsystem Document Tree



3 Technical Specifications Dual Array Controller

This section provides a quick overview of the technical features of the Dual Array Controller.

- PCI based Computer Control and Data Acquisition
 - 3 'Thinserver' platforms
 - Rack mount, rugged low profile form factors
 - 1 Instrument Controller
 - 2 Pixel Servers (1 per array)
 - Compaq Proliant DL360
 - Dual Intel Xeon FC PGA2 processor 3.06/2.8/2.4 GHz
 - Red Hat LINUX OS
 - Built in RAID
 - Systran SL240 2.5Gbps (247MByte/sec) FibreXtreme PCI interface
- Custom 'Cryostat Mounted' Readout Electronics, SDN 3005, 800-230-00
 - 32/16 channel analog clock signal drivers
 - 32 low noise preamplifiers
 - 32 individual 2Mhz 16bit Analog to Digital Converters
 - Systran SL240 2.5Gbps (247MByte/sec) FibreXtreme FPDP interface
 - 2 Embedded Brightstar Engineering IPengine1's
 - 48Mhz PowerPC
 - Altera FPGA
 - ELINUX OS
 - 10BT Ethernet
- Cryostat electronics
 - Integrated array mount/fanout/configuration assembly
 - Cryostat cable assemblies
 - Thermal clamp/light tight feedthroughs
- Low Noise Agilent Switching Power Supply
 - Rack mount, modular
 - Front panel indicators
 - +5VDC,+15VDC, -15VDC for each array
 - Over current, voltage protection

4 Functional and Performance Requirements

This section specifies the functional and performance requirements of the Dual Array Controller. This set of requirements specifies the functionality of the Dual Array Controller.

4.1 High Level Array Control System Functional Requirements

- Must operate two 4 quadrant Aladdin type III style arrays
 - *Reference Document:* SDN 3003 NICI Dual Array Controller
- Must allow synchronization of readouts of the two arrays to 1 millisecond.
 - *'Quick Answer':* The Clocking FPGA circuitry located on the FCRYO2 board will start exposures when in an ARM state and after receiving an opto-coupled TTL level TRIGGER signal. Clocking will be synchronized to within 140nsec.
 - *Reference Document:* FCRYO2 700-200-01
- Single subarray mode minimum size 8x16 placed anywhere in the array and reflected to all four quadrants.
- Global reset
- Single sampled readout mode
- Double correlated sampled readout mode
- Multiple NDR noise reduction sampling mode
 - *'Quick Answer':* The Clocking FPGA circuitry located on the FCRYO2 board allows for flexible clocking encompassing these requirements.
 - *Reference Document:* FCRYO2 700-200-01
- Connect to Gemini through a Socket for remote control
 - State set and state read commands
- Populate the FITS header and ship the data to the DHS
- Must operate in a standalone mode or under Gemini control in a remote mode
- Must provide an image display in standalone mode
- Must provide local storage for standalone mode
 - *Reference Document:* SDN 3003 NICI Dual Array Controller
- Must time stamp frames using Gemini supplied time board
 - *'Quick Answer':* NICI will use a MKIR supplied time board located in the Pixel Servers
 - *Reference Document:* SDN 3003 NICI Dual Array Controller
 - *This requirement has been changed to a Gemini responsibility.*
- Must have macro capability in stand alone mode
 - *Reference Document:* SDN 3003 NICI Dual Array Controller

4.2 High Level Array Control System Performance Requirements

- Read noise - the controller should not increase the device noise by more than 10%
 - *'Quick Answer':* The gain is fixed at X5 and the bandwidth is limited to ~2.9Mhz with resulting calculated noise (with a 1K source impedance) is equal to 53.2uV. For the +/-2.5V input range of the ADCs' one bit (LSB) is equal to 76uV so the preamplifier contributes less than 1 LSB.'
 - *Reference Document:* PREAMP8 700-158-01
 - *'Quick Answer':* The previous generation array controllers using the same analog and ADC circuitry have been able to achieve the read noise requirement on 6 different Aladdin arrays on 3 different telescopes (SUBARU, IRTF, NRL/NO Flagstaff).
- A/D resolution – adequate to get two bits on the noise
 - *'Quick Answer':* The gain is fixed at X5. From experience, the e-/ADU ratio averages ~10e-/ADU at this setting, leaving ~ 4bits of resolution on the noise from single Fowler pair readout of the Aladdin III.
 - *Reference Document:* PREAMP8 700-158-01
- Full frame co-add rate - 2 Hz required (10 Hz goal)
- Full frame to disk rate – 2 Hz required (10 Hz goal)
 - *'Quick Answer':* As of 3/15/2002, testing has that shown data processing and storage rates have achieved the 2 Hz requirement and 10Hz goal for both co-addition and storage.
- Display frame rate stand alone mode – .5 sec to display frame desired.
 - *'Quick Answer':* As of 3/15/2002, no testing has been performed.

5 Functional Description

The Dual Array Controller provides control of and data acquisition from two four-quadrant Aladdin type III 1024x1024 arrays. There is one Redstar3 implementation for each array, Red and Blue. In this implementation, the top and bottom halves of the array are driven separately. The components of each Redstar3 system are four clock/bias boards (CLKBIAS), four 8-channel preamplifier boards (PREAMP8), four 8-channel analog to digital converter boards (ADC8), one fiber interface board (FCRYO2), and an Array Power Supply Subsystem (APSS). The Dual Array Controller interfaces with some peripheral devices. These are the Instrument Controller, Pixel Server Red, Pixel Server Blue, Rack#1's Ethernet Switch, and the Cryostat's Red Array and Blue Array. The Dual Array Controller and its peripheral devices are illustrated in Figure 1.

All of Redstar3 boards are housed in a 63HP Eurocard chassis called an Array Control Chassis.

The following is a description of the flow of commands, control, and data in the Dual Array Controller. The user can interface with the system via the Instrument Control software running in the Instrument Controller via sockets. The connection to the Instrument Controller is through the Rack#1 LAN. The Instrument Controller communicates with the Dual Array Controller via two 10 Base-T fiber interfaces to the FCRYO2 boards to set the arrays' clocking patterns. The Clocker on each of the FCRYO2 boards derives digital clock signals for driving the arrays from the array clocking patterns set by the Instrument Controller. These digital clocks are transmitted across the Clock Control Bus on the backplane to the CLKBIAS boards. The CLKBIAS boards convert the digital clock signals to analog levels. These analog clocks are sent out of the Array Control Chassis on custom Array Control cables to the arrays in the cryostat. The resulting array data outputs are brought back into the Array Control Chassis on the Array Control cables and fed into the PREAMP8 boards. The PREAMP8 boards amplify the array data outputs and send them across the chassis backplane to the ADC8 boards. The ADC8 boards convert the amplified array data outputs to digital format which is pixel data. The 32 pixel data streams are multiplexed onto the Read Data Bus on the backplane and transmitted to the FCRYO2 boards. The pixel data is passed over a 2.5Gbps FPDP fiber link to two server class multiprocessor computers called Pixel Servers. The Pixel Servers can perform preliminary data processing and store the data locally or pass the data on to Gemini's Data Handling System (DHS).

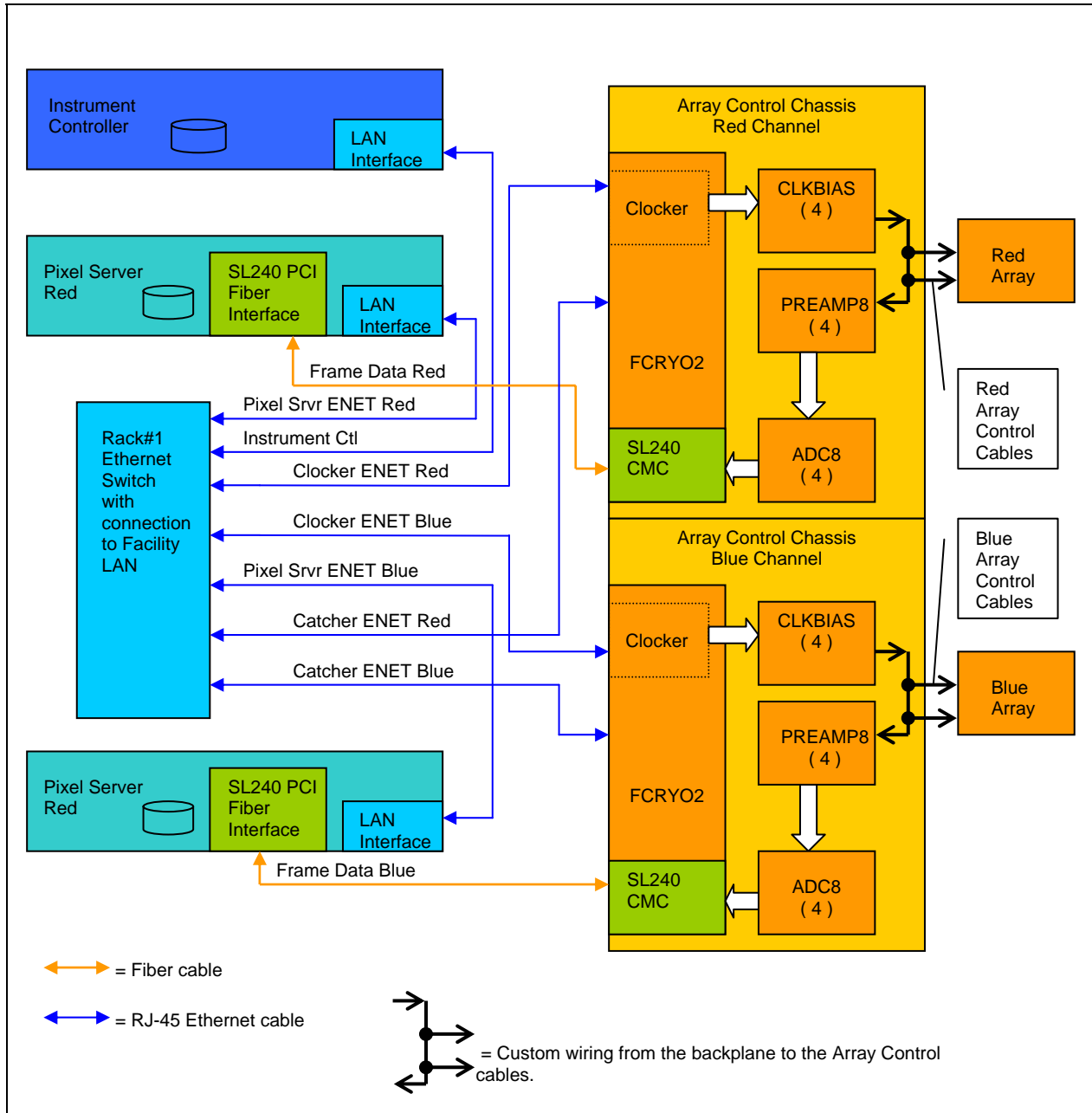


Figure 1 System Level View of the Dual Array Controller

5.1 Array Control Chassis

A Eurocard chassis houses all of the Dual Array Controller’s Redstar3 boards, called the Array Control Chassis. There is one Array Control Chassis which houses all of the boards for the Red and Blue channels.

For each channel there are 15 slots in the front side of the Array Control Chassis numbered from 1 to 15 starting from the left side of the chassis. The naming convention used throughout the documentation does not use this slot numbering scheme. So for this discussion the 15 front side slots are referred to as Apparent Slots. The FCRYO2 board occupies 2 slots, but is only counted as 1 slot. The slot numbering scheme used throughout the documentation refers to this slot numbering scheme. The following table defines the slot locations of all of the boards in the Array Control Chassis.

Slot	Board
1	CLKBIAS VGGCL Configuration, Top half of array.
2	PREAMP8 Top half of array.
3	ADC8 Top half of array.
4	ADC8 Top half of array.
5	PREAMP8 Top half of array.
6	CLKBIAS VDDCL Configuration, Top half of array.
7 – 8	FCRYO2
9	CLKBIAS VGGCL Configuration, Bottom half of array.
10	PREAMP8 Bottom half of array.
11	ADC8 Bottom half of array.
12	ADC8 Bottom half of array.
13	PREAMP8 Bottom half of array.
14	CLKBIAS VDDCL Configuration, Bottom half of array.

Figure 2 Redstar3 Boards’ Slot Assignments

5.1.1 Backplane

The backplane of the Array Control Chassis is based on a standard VME bus with some notable custom differences. There are four 7 slot VME bus cards in the chassis, 2 on the top, 2 on the bottom, for each array channel.

There are 2 connectors for each slot in the chassis. Each connector has 3 columns of 32 pins. When viewed from the front side (the side from which the cards are inserted) the left column of pins is column A, the middle B, the right C. The top connector is referred to as P1 and the bottom is referred to as P2. The P1 portion of the backplane is implemented as the P2 connections are defined in the VME standard, not as P1 is defined in the VME standard. Both the P1 and P2 connectors have shared B column pins with standard termination and custom A and C column connections. That is to say that the B column pins are shared between all slots in the chassis, while the A and C columns are custom wired for each slot.

There are several CLK communication busses in the Array Control Chassis.

- Clock Control Bus: FCRYO2 – CLKBIAS
- Preamp Ribbon Cable: PREAMP8 – ADC8
- Read Data Bus: ADC8 – FCRYO2

The backplane also provides power distribution to all slots in the chassis on the A column of the P1 and P2 connectors. These communication busses and power distribution are described in the following sections.

5.1.1.1 Clock Control Bus

The Clock Control Bus is driven by the FCRYO2 board on the P2 B column, so all boards in the chassis can monitor the Clock Control Bus. The C column of the FCRYO2 board in slot 7 is connected to the B column of slot 8 by a ribbon cable so that the FCRYO2 can drive the Clock Control Bus on the 7 slot backplane for slots 8 – 14. The table below maps P2 B column pins to their corresponding Clock Control Bus signals.

P2	SIGNAL
B1	+5V
B2	DGND
B3	CB_WR!
B4	CB_D0
B5	CB_D1
B6	CB_D2
B7	CB_D3
B8	CB_D4
B9	CB_D5
B10	CB_D6
B11	CB_D7
B12	DGND
B13	+5V
B14	CB_D8
B15	CB_D9
B16	CB_D10
B17	CB_D11
B18	CB_D12
B19	CB_D13
B20	CB_D14
B21	CB_D15
B22	DGND
B23	CB_CW0
B24	CB_CW1
B25	CB_CW2
B26	CB_CW3
B27	CB_CW4
B28	CB_CW5
B29	CB_CW6
B30	CB_CW7
B31	DGND
B32	+5V

Figure 3 Table of Clock Control Bus signals and corresponding P2 pins

5.1.1.2 Read Data Bus

The Read Data Bus is driven by the ADC8 boards on the P1 B column, so all boards in the chassis can monitor the Read Data Bus. The C column of the FCRYO2 board in slot 7 is connected to the B column of slot 8 by a ribbon cable so that the FCRYO2 can monitor the Read Data Bus on the 7 slot backplane for slots 8 – 14. The table below maps P1 B column pins to their corresponding Read Data Bus signals.

P1	SIGNAL
B1	+5V
B2	DGND
B3	RB_RD!
B4	RB_D0
B5	RB_D1
B6	RB_D2
B7	RB_D3
B8	RB_D4
B9	RB_D5
B10	RB_D6
B11	RB_D7
B12	DGND
B13	+5V
B14	RB_D8
B15	RB_D9
B16	RB_D10
B17	RB_D11
B18	RB_D12
B19	RB_D13
B20	RB_D14
B21	RB_D15
B22	DGND
B23	RB_SD0
B24	RB_SD1
B25	RB_SD2
B26	RB_SD3
B27	RB_SD4
B28	RB_SD5
B29	RB_SD6
B30	RB_SD7
B31	DGND
B32	+5V

Figure 4 Table of Read Data Bus signals and corresponding P1 pins

5.1.1.3 Preamp Ribbon Cable

The Preamp Ribbon Cables are driven by the PREAMP8 boards on their P2 connectors' C column. Each PREAMP8 board in the Array Control Chassis has a short ribbon cable connected to the back side of its P2 connector that connects to a neighboring ADC8 board's backside P2 connector. The table below maps P2 Column pins to their corresponding Preamp Ribbon Cable signals. These connections are the same for every PREAMP8 and ADC8 board. P2 C column pins that are not listed in the table are not used for any of the slots containing PREAMP8 or ADC8 boards. **These signal mappings only apply to slots with PREAMP8 and ADC8 boards.**

P2	SIGNAL
C2	AGND
C3	POST1
C4	AGND
C5	POST2
C6	AGND
C7	POST3
C8	AGND
C9	POST4
C10	AGND
C11	POST5
C12	AGND
C13	POST6
C14	AGND
C15	POST7
C16	AGND
C17	POST8
C18	AGND

Figure 5 Table of Preamp Ribbon Cable signals and corresponding P2 pins

5.1.1.4 Power Distribution on the Backplane

Power is supplied to the Array Control Chassis by the Array Power Supply Subsystem via the Array Power Supply cables APS Red and APS Blue. The +5V supplies are distributed over the standard VME locations on the B columns of the P1 and P2 connectors. (Remember, however, that the Array Control Chassis P1 backplane is implemented as P2 is defined in the VME standard.) The +15V and -15V power supplies are distributed on the A columns of the P1 and P2 connectors. The table below indicates the pins which distribute power and ground to all slots.

P1 & P2	SIGNAL
B1	+5V
B2	DGND
B12	DGND
B13	+5V
B31	DGND
B32	+5V

Figure 6 Table of +5V and DGND signals on P1 and P2

P1 & P2	SIGNAL
A1	+15V
A2	AGND
A12	AGND
A22	AGND
A31	AGND
A32	-15V

Figure 7 Table of +15V, -15V and AGND signals on P1 and P2

5.2 Fiber Interface Board, Clocker (FCRYO2)

Each array channel, Red and Blue, utilizes one Fiber Interface Board (FCRYO2). The FCRYO2 provides several functions. First it provides a 10Mbps link to the Instrument Controller (via the Rack#1 Ethernet Switch) for array clocking control. The Instrument Controller writes array clocking patterns to the FCRYO2's embedded Brightstar IP Engine over the Clocker ENET Red or Clocker ENET Blue Ethernet link. These digital clocks are driven over the Array Control Chassis backplane's Clock Control Bus to the CLKBIAS boards. The top and bottom array half's CLKBIAS boards get the functionally equivalent clocking signals. The FCRYO2 also provides a high-speed 2.5Gbps FPDP fiber link (SL240 CMC), Frame Data Red and Frame Data Blue, to the Pixel Servers. Each FCRYO2 board receives two 16 bit pixel data streams over the Read Data Bus from the ADC8 boards. The pixel data is passed over the Frame Data fiber links to two server class multiprocessor computers called Pixel Servers.

The FCRYO2s' Clockers provide the capability to provide synchronized array readouts to within 1 ms. This is accomplished by establishing one of the Clockers to be a master, the other a slave. When the Clockers receive a command from software to begin an array readout the Clockers are armed. The master Clocker waits for a trigger from the customer's system via software ~~the TTL Capture Trigger~~. When the ~~external TTL Capture Trigger~~ trigger is activated, the master Clocker sends an internal synchronization trigger to the slave Clocker over an optocoupled TTL trigger connection. This enables the Red and Blue array readouts to be synchronized to less than 1 ms. The Clockers' clocking patterns and FPGA images are programmed over the Clocker ENET connections.

The FCRYO2 boards' Catchers receive pixel data from the ADC8 boards, buffer them, and send them on to the SL240 CMC fiber interface modules. The Catchers' FPGA images are programmed over the Catcher ENET connections.

The fiber links to the Pixel Servers and Instrument Controller provide optical isolation which allows for ground separation between the Instrument Controller, Pixel Servers, and the Array Control electronics. This helps minimize any noise the Array Controller could introduce into the data streams and the rest of the system.

5.3 Clock Bias (CLKBIAS)

The CLKBIAS boards map digital input control and power signals to analog clock and bias outputs to the arrays. Some array inputs are constant voltage inputs which are driven as bias signals from the CLKBIAS boards. Other array inputs are variable signals, or clocks, which are driven as clock signals from the CLKBIAS boards. There are 2 CLKBIAS boards for each half of each array for a total of 4 per array channel (Red and Blue).

The CLKBIAS board decodes Clock Control Bus sequences from the FCRYO2 boards to generate the analog clock and control signals. These clock and control signals are sent out of the Array Control Chassis over the Array Control cables to the corresponding array in the Cryostat.

There are 19 identical clock and control signals for each array half. Thirteen of the array inputs are clock signals. Each clock signal requires 2 of the CLKBIAS' DACs, one for the clock high voltage, one for the clock low voltage. For each half of the array six of the array inputs are constant voltage, or bias, signals. The bias signals only require one DAC each. Each array half requires 2 CLKBIAS boards for driving all of the control

and power signals to the arrays. One of the CLKBIAS boards for each half is implemented in a VDDCL Configuration for driving 8 of the clock signals. The other CLKBIAS board is implemented in a VGGCL Configuration for driving 5 clock signals and 6 bias signals. For board slot assignments, see Figure 2.

The CLKBIAS boards' bias, high clock, and low clock voltage levels are programmable. The voltages are set to specific levels for each array input signal. The voltages can be set by the user in the Engineering Window of the user interface or can be set by DIP switches on the boards. Selecting between user programmed and DIP switch voltage levels is set by manually shunting two pins on the board for each DAC. The system is shipped configured such that only the VGGCL (DAC0), VDETCOM (DAC10), and VDDUC (DAC11) voltages are programmable. **It is absolutely critical that VDETCOM be set to a more positive voltage than VDDUC or the array can be critically damaged.** Specific voltage settings are available in the CLKBIAS board's specification.

For more details on the CLKBIAS boards, see the board's specification, "CLKBIAS 8/16 CHANNEL CLOCK/BIAS DRIVER BOARD," MKIR# 700-155-01.

5.4 Preamp Boards (PREAMP8)

The PREAMP8 is an 8 channel differential input preamplifier with independent fixed gains (X5). Each amplifier consists of a high impedance input instrumentation amp with shared onboard offset voltage. Array data outputs are routed into the PREAMP8s via the Array Control Chassis' backplane. The PREAMP8 boards amplify the array data outputs and send them across the Clock Bus to the ADC8 boards. Each array quadrant has 8 data outputs, so there are 4 PREAMP8 boards for each array.

The PREAMP8 boards have an offset voltage option on the inputs to the amplifiers. They are configured by an Offset DAC with 12 DIP switch positions for manually setting the offset voltage. The Offset DAC should be set to 0 volts, which corresponds to DIP[11] set high and DIP[10:0] set low.

The PREAMP8 boards also have a voltage reference bias voltage (VREF) option for the current source loads on the inputs to the amplifiers. They are configured by an Offset DAC with 12 DIP switch positions for manually setting the VREF. The VREF DAC should be set to 0 volts, which corresponds to DIP[11] set high and DIP[10:0] set low.

For more details on the PREAMP8, see the board's specification, "PREAMP8 8 Channel Differential Input, Array Optimized Low Noise Preamplifier," MKIR# 700-158-01.

5.5 Analog to Digital Converters (ADC8)

The ADC8 is an 8 channel differential input Analog to Digital Converter board. The ADC8 boards receive amplified analog array data output signals from PREAMP8 boards across the Preamp Ribbon Cable. The ADC8 boards convert the amplified array data outputs to digital format which is pixel data. This pixel data is passed to the FCRYO2 boards over the Read Data Bus on the Array Control Chassis' backplane.

For more details on the ADC8, see the board's specification, "ADC8 8 Channel 2MHz 16 Bit Analog to Digital Converter Board," MKIR # 700-155-01.

5.6 Arrays

In the context of this discussion, Array refers to the MKIR designed Array Mount and the Raytheon 1024 X 1024 InSb Infrared Sensor which is mounted in the Array Mount. There is one array for each channel in NICI, the Red Array and Blue Array. The Array Mount is inside a cryostat. The Array Mount provides connections from the Infrared Sensor to the 61 pin Array Control cables.

For details on the Array Mount see the Array Mount specification.

5.7 Pixel Servers

The main function of the Pixel Servers is image capture. The Pixel Servers gather raw image data from the FCRYO2 boards in the Array Control Chassis and assemble the data into frames, prepare the data for storage, further processing, or human viewing. Having dedicated image processing computers (the Pixel Servers) separate from the Instrument Control computer allows high throughput rates for the data. The Pixel Servers are implemented in Thin Servers. The Thin Server is described in Section 5.9.

The FCRYO2 boards Clocker modules instruct the Pixel Servers to begin capturing a new image object. The raw image that comes off of the arrays is in a non-intuitive, hardware dependent order. The Pixel Servers reassemble the data stream into sequential rows and columns by decoding the clocking pattern used by the FCRYO2's Clocker module to clock the arrays. The decoding sequence is sent to the Pixel Servers by Instrument Controller. The Pixel Servers may also convert the incoming 16 bit pixel data into 32 bit integer or floating point data for optimized CPU processing. The Pixel Servers can perform some preliminary image processing on the data. This includes co-addition, pedestal correction, averaging, flat correction, and flat creation. The data can be tagged with ancillary headers for the DHS or FITS file destinations including NICI filter information and telescope orientation information. Then the data is stored locally or passed on to the DHS.

More specific information about the operation and functionality of the Pixel Servers is available in the document titled "Software Array Control and Image Acquisition for the NICI Instrument".

5.8 Instrument Controller

The Instrument Controller is the main controller of NICI and the Dual Array Controller. The Instrument Controller provides the user interface for all operations in stand-alone and remote modes. The Instrument Controller is implemented in a Thin Server. The Thin Server is described in Section 5.9.

The Instrument Controller provides clocking patterns to the FCRYO2 boards' clocker modules via the Rack#1 LAN. The path is across the Instrument Ctl ENET cable, into the Ethernet Switch, across the Clocker ENET Red and Blue cables to the FCRYO2 boards.

The Instrument Controller also manages the Pixel Servers' image acquisition and processing.

5.9 Thin Servers

To keep the system symmetric and lower maintenance, Redstar3 has standardized on a generic PC form factor for the Pixel Servers and Instrument Controller. This form factor, known as a "Thin Server", intended for the Internet Service Provider market, is a rack mount, high density PC/PCI platform. The Pixel Server and Instrument Controller platforms are of identical hardware (plus or minus disk capacity). The choice of PC platforms versus VME or SPARC is a deliberate attempt to be able to leverage future advancements and the lower price/performance ratios found in the PC market. We have baselined a particular platform for development and testing, a Compaq Proliant DL360 G3. The Pixel Servers and Instrument Controller will be implemented with the DL360 G3. See the attached Appendix for detailed vendor information.

5.9.1 Compaq Proliant DL360 G3 Technical Specifications

This section provides an overview of the technical specifications of the DL360 G3 server.

- Processors: Dual Intel Xeon FC PGA2 processor 3.06/2.8/2.4 GHz
- Memory Standard: 512 MB (PC2100 266MHz 2:1 interleaved ECC DDR SDRAM memory)
- Maximum: 8 GB
- Network Controller: Dual embedded 10/100/1000 Ethernet NIC WOL (Wake On LAN) on separate PCI-X busses.
- Expansion Slots I/O (2 Total) PCI-X Voltage : 2 64-bit /100 MHz PCI 1 3.3 Volt
- Storage Controller: Embedded Smart Array 5i+, with 64 MB memory
 - Note: This controller is embedded on the system board.
 - RAID 0 and RAID 1 capability.
- Storage Diskette Drives 1.44 MB
- CD-ROM 24x IDE CD-ROM Drive (Low-profile, ejectable)
- Maximum Internal Storage 291.2 GB (internal drive cage) (2 x 145.6 GB Wide Ultra3, 1" drives)
- Inter faces:
 - Serial 1
 - Pointing Device (Mouse) 1
 - Graphics 1
 - Hot Plug Keyboard 1
 - USB 2
 - Network RJ-45 2
 - Remote management port 1 Integrated Lights Out (iLO) management port.
- Graphics: Integrated ATI RAGE XL Video Controller with 8-MB SDRAM Video Memory
- Form Factor: Rack (1U), (1.75-in/4.45 cm)



Figure 8 Photo of Compaq Proliant DL360 G3

5.9.2 Systran SL240 PCI, 2.5Gbps Technical Specifications

The Pixel Servers each have a high-speed 2.5Gbps fiber interface to the Redstar3 systems. The interface is implemented in the DL360 servers with a Systran SL240 FibreXtreme Serial FPDP data link card.

- Programmable bi-directional boards provide configuration flexibility
- Minimizes implementation cost and enhances throughput by using a simple protocol
- Two media options available Long wavelength and Short wavelength laser
- End-to-end throughput of up to 247 MB/s without frame checksums
- Built-in data synchronization with minimal on overall data throughput
- Integrated interrupt controller to report transaction completion, or buffer space
- Loop operation with out-of-band arbitration point-to-point operation
- Watchdog timer for failover operation
- Proven 8B/10B encoding for data transmission
- Memory: 1 MB receive buffer, 4 KB transmit
- 64-bit operation is backward compatible 33 MHz
- Status LED that reports link stability
- Hardware Compatibility:
 - PCI Local Bus
 - Specification, Rev. 2.1
 - Physical Dimensions:
 - 4.725" x 4.200" (120.015 mm x 106.680 mm)
 - 50um or 62.5 core fiber
 - ~ 0.25lbs
 - Power dissipation 8.2W average
 - +5VDC, 0.9 Amps av., 1.3 Amps peak
 - +3.3VDC, 1.1 Amps av. and peak



Figure 9 Systran SL240 FibreXtreme Photo

5.10 Array Power Supply Subsystem

The Array Power Supply Subsystem (APSS) is a specially modified HP 66000 series system power supply which supplies the power for the Dual Array Controller. Below are front and rear view photos of the power supplies which illustrate the APSS’s components that are described next.

The APSS houses 6 power modules, 3 for each array. Each array has a +5V, +15V, and –15V module installed in the APSS. Each power module has a corresponding output module on the rear side of the APSS. The output modules’ outputs are connected to the APS cable’s wiring harness. The wiring harness connects to the APS cable which supplies power to one channel (Red or Blue) of the Dual Array Controller. There is one APS cable for each array channel, APS Red and APS Blue.

The custom modifications to the HP66000 are described here. First the modules are programmed to output +5V, +15V, and -15V. The modules are also programmed for over voltage and over current protection such that they shut down in either condition. The HP66000 is also modified to synchronize the power modules outputs via the INHIBIT connector.

Note that the Instrument Controller and Pixel Servers must be powered on before the APSS.

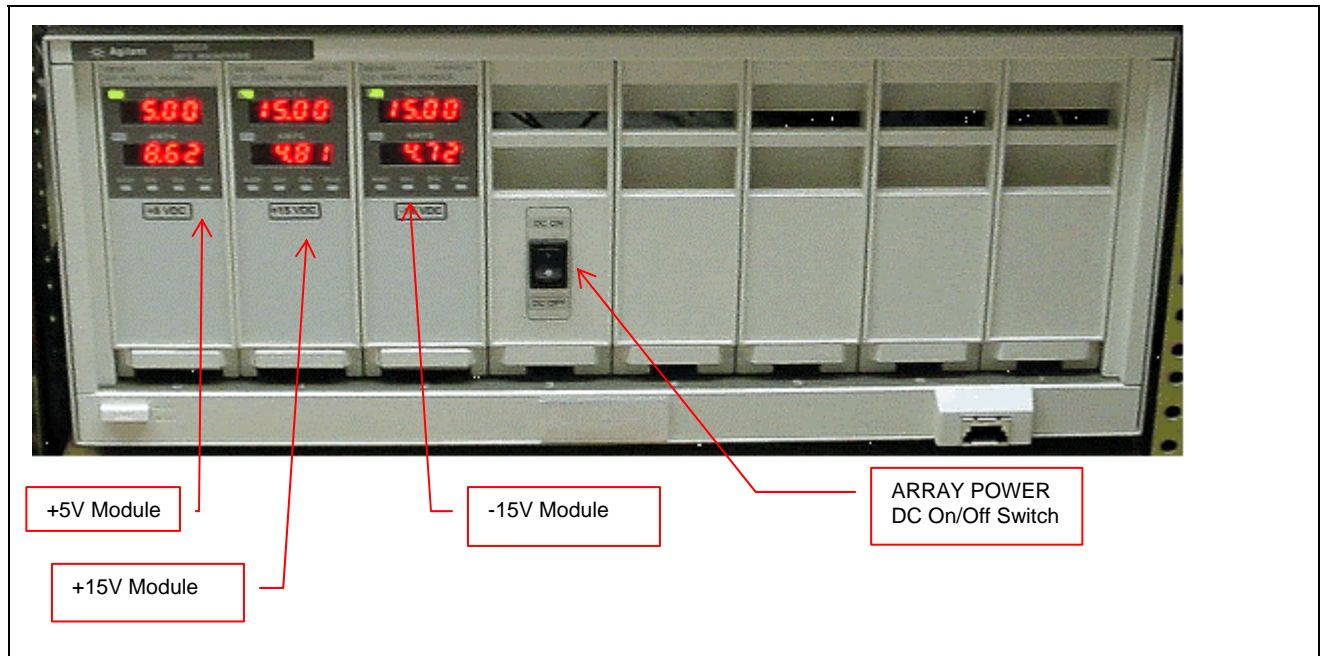


Figure 10 Photo: Array Power Supply Subsystem Front View

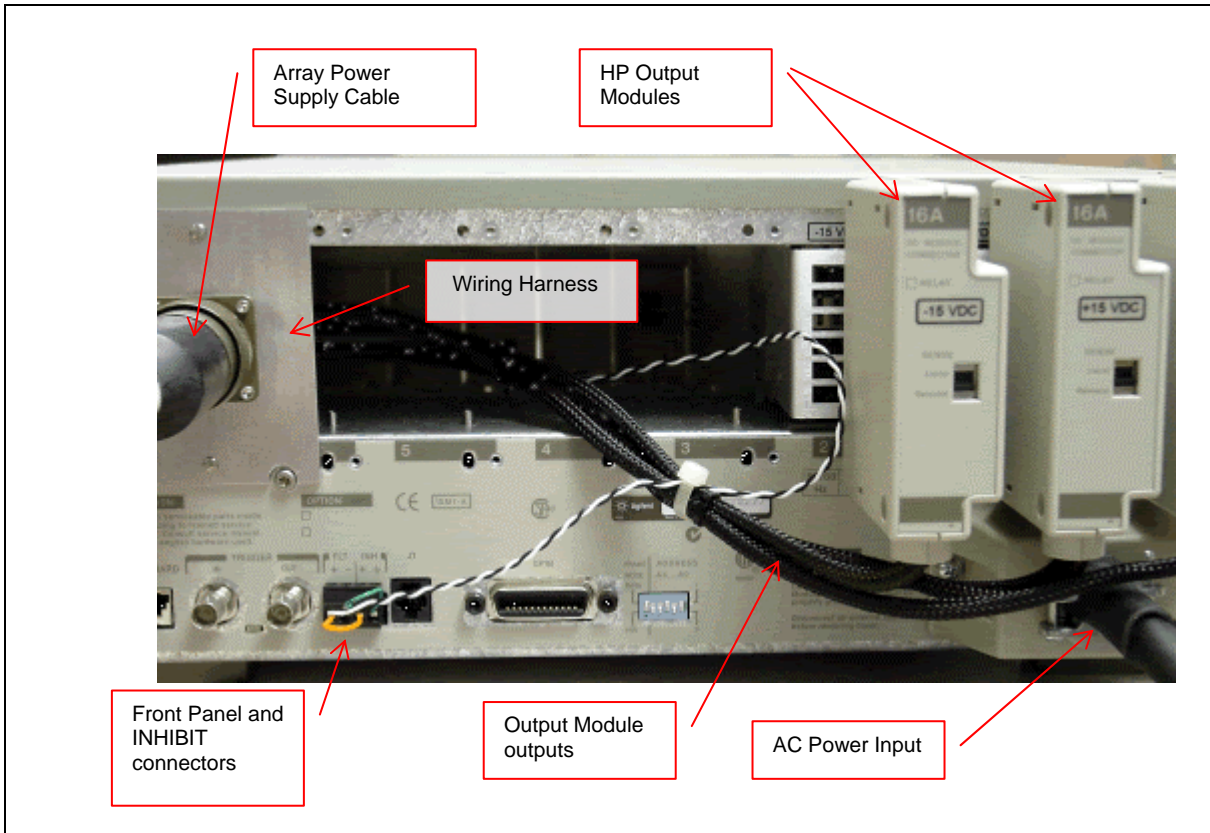


Figure 11 Photo: Array Power Supply Subsystem Rear View

5.10.1 HP Output Module + AC power Installation/Removal

Due to the size of the power supply chassis and shipping crate, the output power modules and AC connector must be removed for shipping. To reinstall the connections, complete the following procedure.

5.10.1.1 AC Power Installation/Removal

To connect the AC power connection to the power supply, confirm that the silver strain relief is loose enough to back the plastic shell off the end of the cable. Connect the BLACK wire to LINE, GREEN to EARTH and WHITE to NEUTRAL. Attach the plastic shell and tighten the strain relief clamp. To disconnect the AC power, reverse the procedure. See the photo below for AC power connection details.

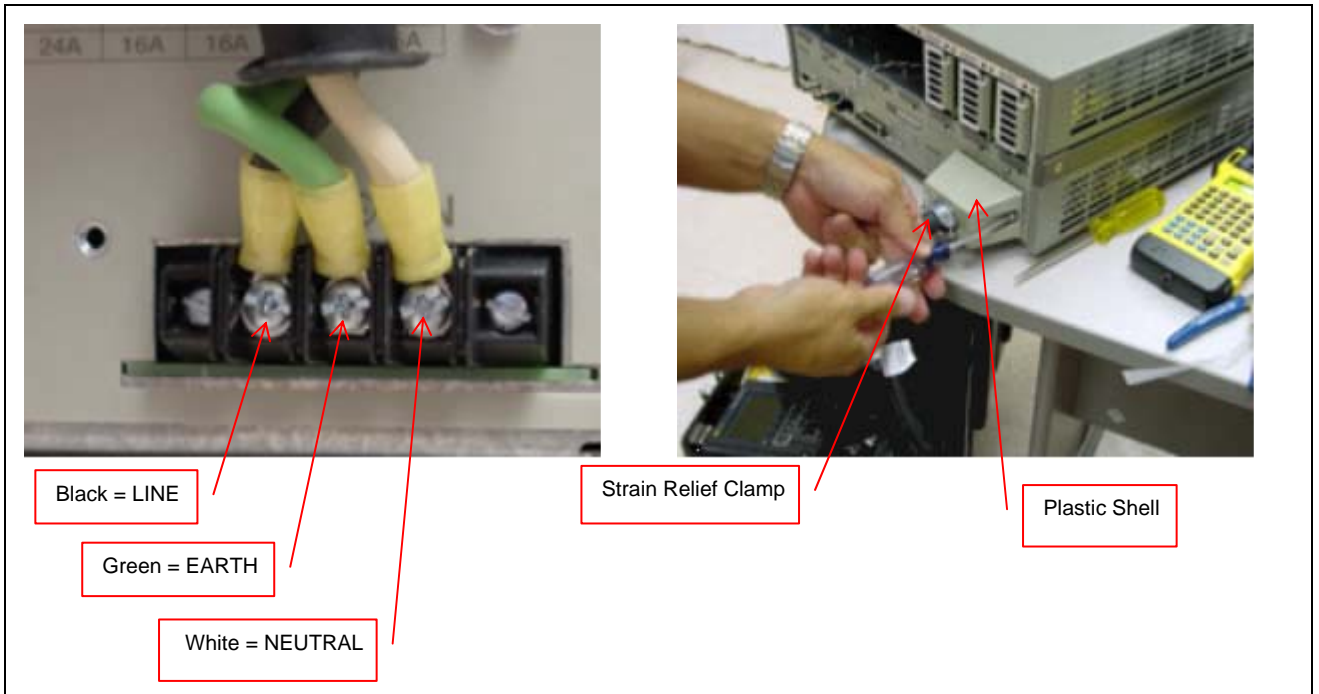


Figure 12 Photo: Array Power Supply Subsystem's AC Power

5.10.1.2 HP Output Module and APS Cable Installation/Removal

A cable harness connects the three HP output modules to the 16 pin panel mount APS cable connector. The APS cable connector should be installed using output module screw holes on the left side of the HP chassis. The 3 output modules (labeled -15VDC, +15VDC, and +5VDC) should be connected to their respective connectors. There are two screws that secure each output module to the APSS chassis.

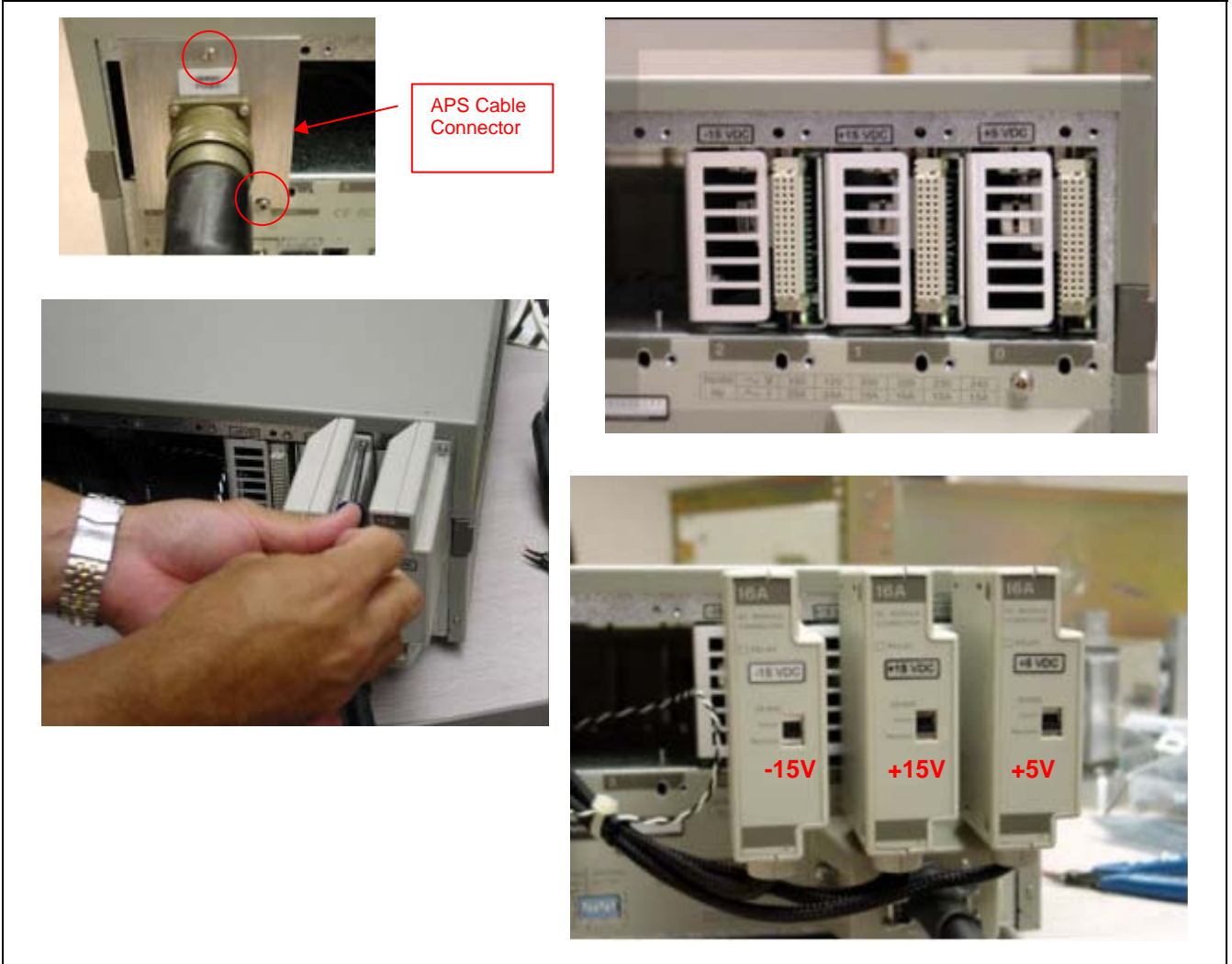


Figure 13 Photos: HP Output Module Installation/Removal

6 System Grounding

The system grounding plan is described in Electronics System Document, MKIR# NICI-900-200-01, Gemini SDN3001. It is crucial that the customer not modify this grounding plan.

7 External Connections and Cabling

This section describes the external interfaces of the Dual Array Controller. A table of all connections and cabling is provided in Figure 14.

Array Control: Connection to the Arrays are made via Glenair custom 61 pin cables specifically designed for low noise, high shielding operation. The Array Control cables are connected to the Cryostat. The cables carry array control, clocking, and data signals. There are 2 Array Control cables for each array, Red Array Ctl 1, Red Array Ctl 2, Blue Array Ctl 1, and Blue Array Ctl 2. The Array Control cables are illustrated in Figure 15.

Clocker ENET: This is an Ethernet connection to Rack#1's Ethernet Switch from the FCRYO2 boards' Clocker modules. This connection permits communication with the Instrument Controller. The Instrument Controller provides clocking configuration to the Clocker module via the Clocker ENET link. There are 2 Clocker ENET connections in the Dual Array Controller, Clocker ENET Red and Clocker ENET Blue.

Catcher ENET: This is an Ethernet connection to Rack#1's Ethernet Switch from the FCRYO2 boards' Catcher modules. This connection permits communication with the Instrument Controller. The Instrument Controller provides FPGA configuration and programming to the Catcher module via the Catcher ENET link. There are 2 Catcher ENET connections in the Dual Array Controller, Catcher ENET Red and Catcher ENET Blue.

Frame Data: A fiber connection from the FCRYO2 boards' to the Pixel Servers for transmitting Frame Data. The connections on the FCRYO2 boards are to the Systran SL240 CMC daughter boards. There are 2 Frame Data connections in the Dual Array Controller, Frame Data Red and Frame Data Blue.

Array Power Supply (APS): The Array Power Supply cable is connected to the Array Power Supply Subsystem. This cable supplies the Array Control Chassis' boards with power. There are 2 APS cables, APS Red and APS Blue.

Cable Name	Manufacturer's Part	# conductors	Type of signals	Connectors
Red Array Ctl 1	Glenair 61 pin ABC56145 rA	61	Critical Low Noise	Cylindrical
Red Array Ctl 2	Glenair 61 pin ABC56145 rA	61	Critical Low Noise	Cylindrical
Blue Array Ctl 1	Glenair 61 pin ABC56145 rA	61	Critical Low Noise	Cylindrical
Blue Array Ctl 2	Glenair 61 pin ABC56145 rA	61	Critical Low Noise	Cylindrical
Clocker ENET Red	RJ-45	2	Optical 10Base-T	ST
Clocker ENET Blue	RJ-45	2	Optical 10Base-T	ST
Catcher ENET Red	RJ-45	2	Optical 10Base-T	ST
Catcher ENET Blue	RJ-45	2	Optical 10Base-T	ST
Frame Data Red	Fiber Optic: Multimode 50/125 μ m multimode fiber (850nm)	2	Optical Frame Data	LC
Frame Data Blue	Fiber Optic: Multimode 50/125 μ m multimode fiber (850nm)	2	Optical Frame Data	LC
APS Red	16-pin Glenair:	16	Power and Ground	Cylindrical
APS Blue	16-pin Glenair:	16	Power and Ground	Cylindrical

Figure 14 Table of External Connections

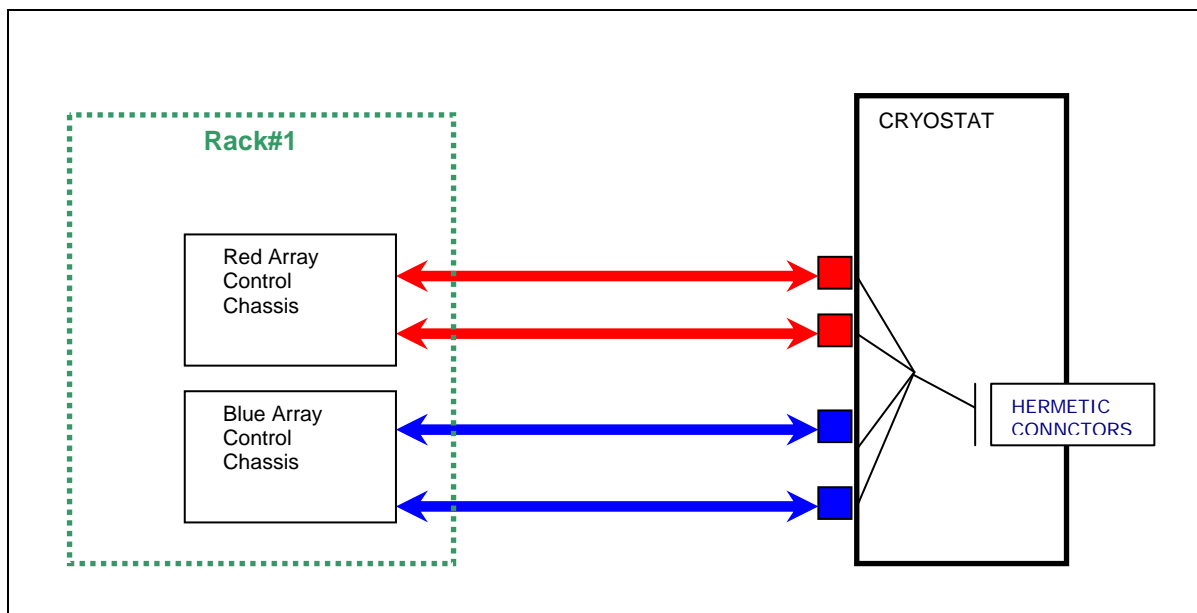


Figure 15 Array Control External Cabling Diagram

8 Acronyms and Definitions

ADC	Analog to Digital Converter
AGND	Analog Ground
AO	Adaptive Optics
Aladdin	A 1024 x 1024 In:Sb 1-5 micron focal plane array.
CCC	Closed Cycle Cooler
DGND	Digital Ground
DHS	Gemini's Data Handling System, a database handler for NICI images.
FCRYO2	Fiber Cryostat Mounted subassembly version 2, a board in the Redstar3
FITS	Flexible Image Transport System, a standard of scientific data storage.
FPDP	Front Panel Data Port. A platform-independent 32-bit synchronous data flow path that allows data to be transferred at high speeds.
FPGA	Field Programmable Gate Array, a programmable integrated circuit.
GND	Electrical ground
HP	Hewlett-Packard
LAN	Local Area Network
LSB	Least Significant Bit
MKIR	Mauna Kea Infrared
NDR	Nondestructive Read